## AMENDMENTS TO THE CLAIMS

WE CLAIM (clean copy)

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (currently amended) A method of performing a k-stage FFT (fast Fourier transform) computation of N data points wherein k and N are integers, the method comprising:

for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, performing a respective plurality of operations on the N data points, each one of the respective plurality of operations comprising:

performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory;

performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory; and

performing an export of the respective plurality of sets of data points of the N data points from the internal memory into the external memory to update the respective plurality of sets of data points of the N data points in the external memory, wherein the stage groupings of at least one stage comprise Q stage groupings each

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comprising S stages, said Q and said S being integers with $Q \geq 1$, $S \geq 1$ and $k \geq QS$, and wherein N substantially satisfies $N = 2^k$, the method further comprising:

grouping, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into $2^{IS}$ blocks of data of $N/2^{IS}$ respective data points;

grouping, within each one of the $2^{IS}$ blocks of data, the $N/2^{IS}$ respective data points into $2^S$ sub-blocks of data of $N/2^{IS+S}$ respective data points;

grouping, within each one of the $2^S$ sub-blocks of data, the $N/2^{IS+S}$ respective data points into $M_1$ sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein $M_1$ is an integer;

taking, within each one of the $2^{IS}$ blocks of data, a respective sub-sub-block of data of the $M_1$ sub-sub-blocks of data from each one of the $2^S$ sub-blocks of data to form a set of $2^S$ sub-sub-blocks of data of $N/(2^{IS}M_1)$ data points a total of $M_1$ times to produce $M_1$ sets of $2^S$ sub-sub-blocks of data of $N/(2^{IS}M_1)$ data points; and

taking, within each one of the $M_1$ sets of $2^S$ sub-sub-blocks of data, a respective data point from each one of the $2^S$ sub-blocks of data to form a set of $2^S$ data points a total of $N/(2^{IS+S}M_1)$ times to produce $N/(2^{IS+S}M_1)$ sets of $2^S$ data points.

10. (original) A method of performing a k-stage FFT computation according to claim 9 wherein, for the stage grouping, I, of the of the Q stage groupings of the plurality of stage groupings, the performing a respective plurality of operations on the N data points comprises performing $M_1$ of the plurality of operations for each one of the $2^{IS}$ blocks of data within the stage grouping, I, each one of the $M_1$ of the plurality operations comprising:

performing an import of respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points from the external memory into the internal memory;

performing an S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points in the internal memory; and

performing an export of the respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points from the internal memory into the external memory to update the respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points in the external memory.

11. (original) A method of performing a k-stage FFT computation according to claim 10 wherein $M_I$ substantially satisfies $M_I = N/(2^{IS}M_I)$ wherein $M_I$ corresponds to the number of data points the internal memory can hold.

12. (original) A method of performing a k-stage FFT computation according to claim 10 wherein $M_I$ substantially satisfies $M_I = N/(2^{IS-1}M_I)$ wherein $M_I$ corresponds to the number of data points a buffer in the internal memory can hold.

13. (original) A method of performing a k-stage FFT computation according to claim 10 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points results in $N/(2^{IS+S} M_I)$ S-stage FFT computations, the $N/(2^{IS+S} M_I)$ S-stage FFT computations comprising performing one stage of S stages for each one of the $N/(2^{IS+S} M_I)$ S-stage FFT computations and iterating through the S stages.

14. (original) A method of performing a k-stage FFT computation according to claim 10 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points results in $N/(2^{IS+S} M_I)$ S-stage FFT computations, the $N/(2^{IS+S} M_I)$ S-stage FFT computations comprising performing computations for S stages of an S-stage FFT computation of one of the $N/(2^{IS+S} M_I)$ S-stage FFT computations before another S-stage FFT computation is performed on another of one of the $N/(2^{IS+S} M_I)$ S-stage FFT computations.

15. (canceled)

16. (canceled)

17. (canceled)

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19. (canceled)

20. (canceled)

21. (canceled)

22. (canceled)

23. (canceled)

24. (canceled)

25. (canceled)

26. (currently amended) A processor comprising:

an internal memory adapted to store data;

a DMA (direct memory access) unit adapted to import data into the internal memory and to export data from the internal memory; and

a central processor unit (CPU) adapted to perform, for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, a respective plurality of operations on the N data points, for each one of the respective plurality of operations the CPU is adapted to:

provide instructions to the DMA unit for performing an import of a respective plurality of sets of data points, of N data points, into the internal memory;

perform a FFT computation upon each one of the respective plurality of sets of data points, of the N data points, in the internal memory; and

provide instructions to the DMA unit for performing an export of the respective plurality of sets of data points, of the N data points, from the internal memory to update the respective plurality of sets of data points of the N data points, wherein the CPU is adapted to:

group, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into $2^{IS}$ blocks of data of $N/2^{IS}$ respective data points;

group, within each one of the $2^{IS}$ blocks of data, the $N/2^{IS}$ respective data points into $2^S$ sub-blocks of data of $N/2^{IS+S}$ respective data points;

group, within each one of the $2^S$ sub-blocks of data, the $N/2^{IS+S}$ respective data points into $M_I$ sub-sub-blocks of data of $N/(2^{IS+S} M_I)$ respective data points wherein $M_I$ is an integer;

take, within each one of the $2^{IS}$ blocks of data, a respective sub-sub-block of data of the $M_I$ sub-sub-blocks of data from each one of the $2^S$ sub-blocks of data to form a set of $2^S$ sub-sub-blocks of data of $N/(2^{IS}M_I)$ data points a total of $M_I$ times to produce $M_I$ sets of $2^S$ sub-sub-blocks of data of $N/(2^{IS}M_I)$ data points; and

take, within each one of the $M_I$ sets of $2^S$ sub-sub-blocks of data, a respective data point from each one of the $2^S$ sub-blocks of data to form a set of $2^S$ data points a total of $N/(2^{IS+S}M_I)$ times to produce $N/(2^{IS+S}M_I)$ sets of $2^S$ data points.

27. (original) A processor according to claim 26 wherein, for the stage grouping, I, of the of the Q stage groupings of the plurality of stage groupings, the CPU is adapted to perform $M_I$ of the plurality operations for each one of the $2^{IS}$ blocks of data within the stage grouping, I, and for each one of the $M_I$ of the plurality operations the CPU is adapted to:

provide instructions to the DMA unit for performing an import of respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points into the internal memory;

performing an S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points in the internal memory; and

provide instructions to the DMA unit for performing an export of the respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points from the internal memory to update the respective $N/(2^{IS+S}M_I)$ sets of $2^S$ data points.

28. (original) A processor according to claim 27 wherein the internal memory comprises a buffer adapted to store the plurality of sets of data points, wherein the buffer has a capacity to hold $M_I$ data points and $M_I$ substantially satisfies $M_I = N/(2^{IS}M_I)$ wherein $M_I$ in an integer.

29. (original) A processor according to claim 27 wherein the internal memory comprises a double buffer adapted to store the plurality of sets of data points, wherein the double buffer comprises two buffers each capable of storing $M_I/2$ data points and wherein said $M_1$ substantially satisfies $M_1 = N/(2^{IS-1}M_I)$, $M_I$ being an integer.

30. (original) A processor according to claim 29 wherein while the CPU performs the S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points, the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points being stored in one of the two buffers, the CPU is adapted to provide instructions to the DMA unit to import, into another one of the two buffers, respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points of a next one of the each one of the $M_1$ of the plurality operations.

31. (original) A processor according to claim 29 wherein while the CPU performs the S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points, the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points being stored in one of the two buffers, the CPU is adapted to provide instructions to the DMA unit to export, from another one of the two buffers, respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points from previous one of the each one of the $M_1$ of the plurality operations.

32. (original) A processor according to claim 27 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points results in $N/(2^{IS+S}\ M_1)$ S-stage FFT computations, the CPU being further adapted to evaluate the $N/(2^{IS+S}\ M_1)$ S-stage FFT computations at one stage of S stages for each one of the $N/(2^{IS+S}\ M_1)$ S-stage FFT computations and iterate through the S stages.

33. (original) A processor according to claim 27 wherein the internal memory comprises a high-speed cache.

34. (original) A processor according to claim 33 wherein the performing an S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points results in $N/(2^{IS+S}\ M_1)$ S-stage FFT computations, the CPU being further adapted to perform computations for S stages of an S-stage FFT computation of one of the $N/(2^{IS+S}\ M_1)$ S-stage FFT computations

before performing another S-stage FFT computation of another one of the $N/(2^{IS+S} M_I)$ S-stage FFT computations.

35. (original) A processor according to claim 28 wherein the stage groupings of at least one stage comprise a stage grouping of D stage wherein D is an integer, said k substantially satisfying k=QS+D and said D substantially satisfying $D \leq \log_2(M_I)$.

36. (original) A processor according to claim 29 wherein the stage groupings of at least one stage comprise a stage grouping of D stage wherein D is an integer, said k substantially satisfying k=QS+D and said D substantially satisfying $D \leq \log_2(M_I/2)$.

37. (canceled)

38. (canceled)

39. (canceled)

40. (canceled)

41. (currently amended) An article of manufacture comprising:

a computer usable medium having computer readable program code means embodied therein for performing a k-stage FFT computation of N data points wherein k and N are integers, the computer readable code means in said article of manufacture comprising:

computer readable code FFT means for performing, for each one of a plurality of stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages, a respective plurality of operations on the N data points, for each one of the respective plurality of operations the computer readable code FFT means comprising:

computer readable code means for providing instructions for performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory;

computer readable code means for performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory; and

computer readable code means for providing instructions for performing an export of the respective plurality of sets of data points of the N data points from the internal memory into the external memory to update the respective plurality of sets of data points of the N data points in the external memory, wherein the stage groupings of at least one stage comprise a stage grouping of D stage and Q stage groupings of S stages wherein D, Q and S are integers and wherein said k substantially satisfies $k=QS+D$ and $k = \log_2(N)$, the article of manufacture comprising further computer readable code means for:

grouping, within a stage grouping, I, of the Q stage groupings wherein I is an integer satisfying $0 \leq I \leq Q-1$, the N data points into $2^{IS}$ blocks of data of $N/2^{IS}$ respective data points;

grouping, within each one of the $2^{IS}$ blocks of data, the $N/2^{IS}$ respective data points into $2^S$ sub-blocks of data of $N/2^{IS+S}$ respective data points;

grouping, within each one of the $2^S$ sub-blocks of data, the $N/2^{IS+S}$ respective data points into $M_1$ sub-sub-blocks of data of $N/(2^{IS+S} M_1)$ respective data points wherein $M_1$ is an integer;

taking, within each one of the $2^{IS}$ blocks of data, a respective sub-sub-block of data of the $M_1$ sub-sub-blocks of data from each one of the $2^S$ sub-blocks of data to form a set of $2^S$ sub-sub-blocks of data of $N/(2^{IS}M_1)$ data points a total of $M_1$ times to produce $M_1$ sets of $2^S$ sub-sub-blocks of data of $N/(2^{IS}M_1)$ data points; and

taking, within each one of the $M_1$ sets of $2^S$ sub-sub-blocks of data, a respective data point from each one of the $2^S$ sub-blocks of data to form a set of $2^S$ data points a total of $N/(2^{IS+S}M_1)$ times to produce $N/(2^{IS+S}M_1)$ sets of $2^S$ data points.

42. (original) An article of manufacture according to claim 41 wherein, for the stage grouping, I, of the of the Q stage groupings of the plurality of stage groupings, the computer readable code FFT means is further adapted to perform $M_1$ of the plurality operations for each one of the $2^{IS}$ blocks of data within the stage grouping, I, and for

each one of the $M_1$ of the plurality operations the computer readable code FFT means further comprising:

computer readable code means for providing instructions for performing an import of respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points from the external memory into the internal memory;

computer readable code means for performing an S-stage FFT computation of the k-stage FFT computation upon each set of $2^S$ data points of the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points in the internal memory; and

computer readable code means for providing instructions for performing an export of the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points from the internal memory into the external memory to update the respective $N/(2^{IS+S}M_1)$ sets of $2^S$ data points in the external memory.

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